Active Circuits With Diodes: Topological Conditions Sufficient to Determine the State of a Diode

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***Abstract*— Let N be a circuit composed of a finite number of positive and negative linear resistors, ideal diodes, nullators, norators and independent current and voltage sources. In this article, we consider the problem to determine, without any numerical computation, the state of a diode of N. We propose a set of topological conditions such that, when verified by a diode of N, the state of the diode is determined and the same in all the solutions of N. Our results may simplify, sometimes dramatically, the usual trial-and-error procedure to find the solutions of N.**

***Index Terms*— Nonlinear circuits, resistive circuits, active circuits, ideal diodes, piecewise linear circuits, dc analysis, topological conditions.**

I. Introduction

IN THIS article we consider circuits composed of a finite number of positive linear resistors, negative linear resistors, ideal diodes, nullators and norators (usually, but not necessarily, in equal number), and nonzero independent voltage and current sources. We assume, without loss of generality, that the values of all the sources are *positive*.

The symbols and the reference directions adopted for the current and voltage for each component are represented in Fig. 1. Let us observe that the reference directions adopted for the current and voltage sources are *not* the usual associated reference directions. The constitutive relation for each ideal diode is:

$$v \leqslant 0, \quad i \geqslant 0, \quad vi = 0$$

A *solution* of a circuit N is a pair $(\mathbf{i}, \mathbf{v}) \in \mathbf{R}^\rho \times \mathbf{R}^\rho$, where ρ is the number of branches of N, such that the column $\mathbf{i}$ of the *branch currents* and the column $\mathbf{v}$ of the *branch voltages* verify *Kirchhoff's Laws* and the *constitutive relation* of each component. The set of all the solutions of N will be denoted by $S(N)$. Of course, if N has no solution, then $S(N)$ is the empty set.

Let $\mathbf{s} \in S(N)$. We say that a diode of N "is in the *open state* in $\mathbf{s}$" (resp.: "is in the *closed state* in $\mathbf{s}$") if the current i and the voltage v of the diode, in $\mathbf{s}$, are such that $i = 0$ and $v \leqslant 0$ (resp.: $v = 0$ and $i \geqslant 0$). Let us observe that, if D is a diode of N, the statements "the diode D is in the open state in $\mathbf{s}$" and "the diode D is in the closed state in $\mathbf{s}$" are both correct if and only if, in $\mathbf{s}$, it is both $i = 0$ and $v = 0$.

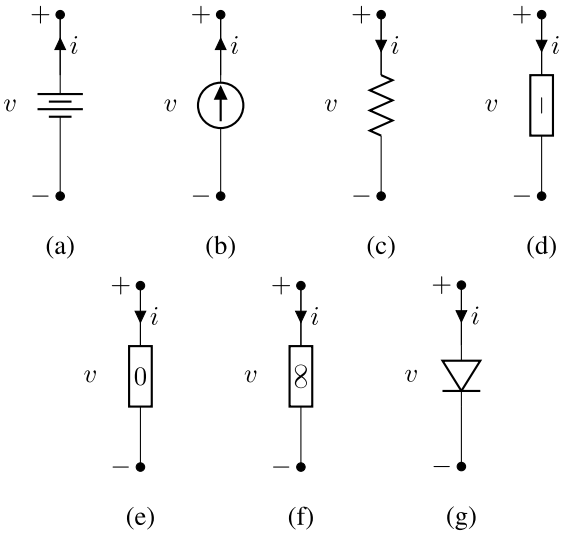

Fig. 1. Symbols and reference directions: (a) voltage source, (b) current source, (c) positive linear resistor, (d) negative linear resistor, (e) nullator, (f) norator, (g) diode.

Let N be a circuit and let $d \geqslant 1$ be the number of ideal diodes in N. A general and elementary procedure to find $S(N)$ is the following [1, Section 16.3.1], [2, Section 2-7], [3, Example 4.2]:

For each of the 2^d combinations of states of the diodes, *repeat*:

(a) replace in N each open diode by an open circuit and each closed diode by a short circuit, and find the solution set of the *linear* circuit obtained,

(b) among these solutions, find those consistent with the combination of states of the diodes under consideration.

Obviously, if no solution is found, then N has no solution, otherwise each of the solutions found is a solution of N, and every solution of N is found in this way.

A drawback of this procedure is its complexity, *exponential* in the number d of diodes. The exponential complexity is essentially due to the fact that, despite the procedure being very familiar in electronic textbooks, no *simple and rigorous technique* has been found *to predict the state*, open or closed, of some of the diodes of N (*to predict the state of a diode* D *of* N *to be open* [resp. *closed*] means: to establish, *without any numerical computation*, that if $\mathbf{s}$ is

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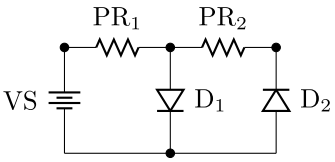

Fig. 2. Circuit N of Example 1.

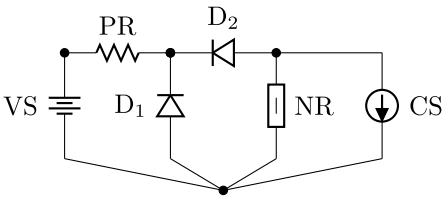

Fig. 3. Circuit N of Example 2 and of Example 3 of Section IV.

a solution of N, then the diode D is in the open [resp. closed] state in $\mathbf{s}$). Indeed, only to mention two very good and widespread electronics textbooks, the unique technique suggested to predict the state of some of the diodes is by an *educated guess* driven by experience [2, p. 53], or by practice [4, p. 103-104].

The aim of this article is to provide some simple *topological conditions*, sometimes applicable by inspection, *sufficient* to predict the state of some diodes of N. By their topological nature, the conditions are independent of the actual value of the resistances and sources.

To understand how our results may be used to reduce the complexity of the elementary procedure, let us consider the following two simple examples.

Example 1: Let N be the circuit of Fig. 2, and let $R_1 > 0$, $R_2 > 0$ and $E > 0$ be the value of the resistance of the positive linear resistors $\mathrm{PR}_1, \mathrm{PR}_2$, and of the voltage source VS, respectively. Let v_1 and i_1 (resp. v_2 and i_2) be the voltage and current of D_1 (resp. D_2).

Using either Theorem 2 or Corollary 1 of Section III, we can predict the state of the diode D_1 to be *closed* and the state of D_2 to be *open*. This means that either N has no solution, or *for every solution* $\mathbf{s}$ of N, in D_1 the current is $i_1 \geqslant 0$ and the voltage is $v_1 = 0$, and in D_2 the current is $i_2 = 0$ and the voltage is $v_2 \leqslant 0$.

To find all the solutions of N, it is now *sufficient* to analyse only *one* linear circuit, L, instead of the 2^2 required by the elementary procedure: the circuit obtained by replacing in N the diode D_1 by a short circuit and D_2 by an open circuit.

The linear circuit L has a unique solution, $\mathbf{s}$, and in $\mathbf{s}$ it is:

$$v_1 = 0, \quad i_1 = E/R_1$$

and:

$$v_2 = 0, \quad i_2 = 0$$

For every positive value of the resistances and source, this solution is consistent with the combination of states of the diodes, hence N has a unique solution.

Observe that, in $\mathbf{s}$, the diode D_2 is *both* in the open *and* in the closed state. Hence $\mathbf{s}$ is *also* a solution, consistent with the combination of states of the diodes, of the linear circuit obtained assuming both D_1 and D_2 in the closed state.

Example 2: Let N be the circuit of Fig. 3, and let $R > 0$, $R^* < 0$, $E > 0$ and $J > 0$ be the value of the resistance of the positive linear resistor PR, of the resistance of the negative linear resistor NR, of the voltage source VS and of the current source CS, respectively. Let v_1 and i_1 (resp. v_2 and i_2) be the voltage and current of D_1 (resp. D_2).

Using Theorem 1 of Section II, we can predict the state of the diode D_1 to be *open*. This means that either N has no solution, or *for every solution* $\mathbf{s}$ of N, in D_1 the current is $i_1 = 0$ and the voltage is $v_1 \leqslant 0$.

To find all the solutions of N, it is now *sufficient* to analyse only *two* linear circuits instead of the 2^2 required by the elementary procedure. The first linear circuit, L_1, is that obtained by replacing in N the diode D_1 by an open circuit and D_2 by a short circuit. The second linear circuit, L_2, is that obtained by replacing in N the diode D_1 again by an open circuit and D_2 by an open circuit.

For the linear circuit L_1, we have three different cases:

(1) *If* $R + R^* \neq 0$, *then* L_1 has a unique solution, $\mathbf{s}'$, and in $\mathbf{s}'$ it is:

$$v_1' = \frac{R^*}{R + R^*}(RJ - E), \quad i_1' = 0$$

and:

$$v_2' = 0, \quad i_2' = -\frac{E + R^*J}{R + R^*}$$

(2) *If* $R + R^* = 0$ and $E + R^*J = 0$, *then* L_1 has an infinite number of solutions. Precisely, for every $\alpha \in \mathbf{R}$ there is a unique solution, $\mathbf{s}_\alpha$, and in $\mathbf{s}_\alpha$ it is:

$$v_{\alpha,1} = -(R\alpha + E), \quad i_{\alpha,1} = 0$$

and:

$$v_{\alpha,2} = 0, \quad i_{\alpha,2} = \alpha$$

(3) *If* $R + R^* = 0$ and $E + R^*J \neq 0$, *then* L_1 has no solutions.

The linear circuit L_2, for every value of the components, has a unique solution, $\mathbf{s}''$, and in $\mathbf{s}''$ it is:

$$v_1'' = -E, \quad i_1'' = 0$$

and:

$$v_2'' = -(E + R^*J), \quad i_2'' = 0$$

The actual number of solutions of N depends on the value of the components.

For example, let $R = 1\Omega$ and $R^* = -2\Omega$, so that $R + R^* \neq 0$.

If $E = 3\mathrm{V}$ and $J = 1\mathrm{A}$, then we have:

$$v_1' = -4, \quad i_1' = 0, \quad v_2' = 0, \quad i_2' = 1$$

and:

$$v_1'' = -3, \quad i_1'' = 0, \quad v_2'' = -1, \quad i_2'' = 0$$

Both $\mathbf{s}'$ and $\mathbf{s}''$ are consistent with the combination of states of the diodes, hence N has *two* solutions. The state of D_1 is

open in both solutions, and the state of D_2 is closed in $\mathbf{s}'$, and open in $\mathbf{s}''$.

If $E = 1\text{V}$ and $J = 1\text{A}$, then we have:

$$v_1' = 0, \quad i_1' = 0, \quad v_2' = 0, \quad i_2' = -1$$

and:

$$v_1'' = -1, \quad i_1'' = 0, \quad v_2'' = 1, \quad i_2'' = 0$$

Both $\mathbf{s}'$ and $\mathbf{s}''$ are *not* consistent with the combination of states of the diodes, and N has *no solutions*.

If $E = 2\text{V}$ and $J = 1\text{A}$, then we have $\mathbf{s}' = \mathbf{s}''$ and:

$$v_1' = -2, \quad i_1' = 0, \quad v_2' = 0, \quad i_2' = 0$$

In this case, $\mathbf{s}'$ is consistent both with the combination of states of the diodes relative to L_1 and with the combination of states of the diodes relative to L_2. Hence N has *only one* solution, in which the state of D_1 is open and the state of D_2 is both open and closed.

Finally, let $R = 1\Omega$, $R^* = -1\Omega$, $E = 1\text{V}$ and $J = 1\text{A}$. In this case it is $R + R^* = 0$ and $E + R^*J = 0$. Then:

(i) for every $\alpha \in \mathbf{R}$ the circuit L_1 has a unique solution, $\mathbf{s}_\alpha$, and in $\mathbf{s}_\alpha$ it is:

$$v_{\alpha,1} = -(\alpha + 1), \quad i_{\alpha,1} = 0$$

and:

$$v_{\alpha,2} = 0, \quad i_{\alpha,2} = \alpha$$

(ii) in the unique solution of the circuit L_2 it is:

$$v_1'' = -1, \quad i_1'' = 0, \quad v_2'' = 0, \quad i_2'' = 0$$

In this case:

(a) the solution $\mathbf{s}_\alpha$ of L_1 is consistent with the combination of states of the diodes if and only if $\alpha \geqslant 0$,

(b) the solution of L_2 is consistent with the combination of states of the diodes.

Hence N has *an infinite number* of solution and for every $\mathbf{s} \in S(N)$ the state of D_1 is open and the state of D_2 is closed in $\mathbf{s}$.

For the same class of circuits considered in the present paper, Fosséprez, Hasler and Schnetzler discovered, in [5], a subtle and deep topological condition necessary and sufficient to identify the combinations of states of the diodes such that, for every value of the resistances and sources, the related linear circuit has no solutions consistent with the states of the diodes. This result can be used to determine, without any numerical computation, *the minimum set* of linear circuits to be solved in the elementary procedure: each of the linear circuits corresponding to combinations of states satisfying the topological condition, *must not* be solved, and all the remaining linear circuits *must* be solved. Unfortunately, to determine all the solutions of N with this technique, apart from the solution of the minimum number of linear circuits, the topological check must be repeated *for each* of the 2^d combinations of states, i.e. 2^d *times*. Then, even if the number of linear circuits to solve has been minimized, there is *no reduction of complexity*.

Some more favorable results are known for circuits composed of positive linear resistors, ideal diodes and independent voltage and current sources (i.e.: without active components). In [6], the authors proved a simple condition sufficient to predict the state of a diode. Precisely, if the diode is part of a suitable loop (resp.: of a suitable cut-set) then it is in the closed (resp.: open) state. This result is attractive, but it can be applied *only* if the circuit is a one-port composed by ideal diodes, short circuits, and open circuits, excited by an independent voltage source in series with a positive linear resistor. Finally, in [7] we proved three pairs of topological conditions sufficient to predict the state of a diode; these results are summarized, and slightly improved, in Section III.

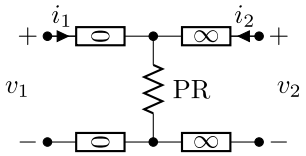

Fig. 4. A two-port equivalent to a VCCS, and its constitutive equations. $R > 0$ is the resistance of PR.

The results of the present paper are attractive, with respect to those allowed by [5], because our topological condition concerns *the state of each of the diodes of the circuit, one at a time*. Whenever one of the diodes verifies the condition, i.e. the state of the diode has been predicted, we avoid, *in one shot*, the solution of all the linear circuits related to the combinations of states in which the diode has not the predicted state: we *halve* the number of linear circuits to be solved to find all the solutions of N. This property allows us, as shown in Section V, to obtain a procedure, to find the solutions of N, in which our topological check must be repeated, at worst, *only* $d(d+1)/2$ *times*, and $2^{d-\delta}$ linear circuits must be solved, where δ is the number of diodes whose state has been predicted.

Remark 1: Our results can be applied to any circuit composed of a finite number of multiport or multiterminal elements, as long as each of such elements is equivalent to the connection of a finite number of positive linear resistors, negative linear resistors, ideal diodes, nullators, norators, and independent voltage and current sources. For example, in Fig. 4 it is shown a two-port composed of two nullators, two norators and one positive linear resistor, equivalent to a voltage controlled current source (VCCS). Similar equivalent circuits for all the linear controlled sources and also for other linear active elements can be found in [8], and for some nonlinear one-ports in [9, Sect. 3.1 and 3.2]. An example of application of our results to the analysis of a circuit containing nonlinear one-ports of the above kind, is given in Example 5 of Section IV, where for each diode of the circuit the *constant-voltage-drop* model is adopted.

The paper is structured as follows: in Section II, we propose our set of conditions. In Section III, we consider the particular case of circuits composed of positive linear resistors, ideal diodes and nonzero independent sources, and we summarize and slightly improve our previous results of [7]. In Section IV, we propose some simple examples to show how our conditions can be used iteratively to analyse a circuit, and also to analyse circuits in which, for the diodes, a more complex model than the ideal one has been adopted. In Section V we summarize

our results and we outline the first steps of our future work. In the Appendix we state and prove a lemma used in the proof of Corollary 1.

II. The Topological Conditions

This section contains our main results concerning circuits with *active components*.

Let N be a circuit. A *loop of elements of type* $X_1, \ldots, X_k$ (resp.: a *cut-set of elements of type* $X_1, \ldots, X_k$) is a loop (resp.: a cut-set) of N whose elements can be partitioned into k disjoint subsets $S_1, \ldots, S_k$ – each one may be empty – such that: for $j = 1, \ldots, k$, the set S_j contains *only* elements of type X_j.

The following definition introduces the *topological* notions necessary to state our results.

Definition 1: Let N be a circuit.

A *loop* (resp.: a *cut-set*) of N is *admissible* if all the diodes in the loop (resp.: in the cut-set), oriented as the reference direction of the current, have the same orientation in the loop (resp.: in the cut-set).

Let D be a diode, S be an independent source, and α be a loop or a cut-set of N.

The diode D and the source S are *equi-oriented in* α (resp.: *anti-oriented in* α) if: α contains both D and S, and the elements D and S, oriented as the reference direction of the current, have the same orientation in α (resp.: have the opposite orientation in α).

Finally, let α be a loop (resp.: a cut-set) of N containing D. Define the following partition of the elements of α:

P_α: the set of all the *positive* linear resistors, and of all the independent voltage (resp.: current) sources S_k such that S_k and D are *anti-oriented* in α;

N_α: the set of all the *negative* linear resistors, and of all the independent voltage (resp.: current) sources S_k such that S_k and D are *equi-oriented* in α;

Z_α: the set of all the diodes, and of all the nullators;

I_α: the set of all the independent current (resp.: voltage) sources, and of all the norators.

We can now state and prove our main result.

Theorem 1: Let N be a circuit containing at least one diode, and let D be one of the diodes of N. The following statements hold:

(1_a) *If* D is part of an admissible loop of diodes and nullators, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *closed* state in $\mathbf{s}$;

(1_b) Let D be not part of a loop as in (1_a), and let $\mathscr{M}$ be the set of all the admissible loops μ containing D and such that:

(i) μ contains no nullators and for every current source CS in μ, D and CS are equi-oriented in μ;

(ii) it is: $(I_\mu \neq \varnothing)$ or $(P_\mu \neq \varnothing$ and $N_\mu \neq \varnothing)$

If the set $\mathscr{M}$ is empty, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *open* state in $\mathbf{s}$;

(2_a) *If* D is part of an admissible cut-set of diodes and nullators, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *open* state in $\mathbf{s}$;

(2_b) Let D be not part of a cut-set as in (2_a), and let $\mathscr{T}$ be the set of all the admissible cut-sets θ containing D and such that:

(i) θ contains no nullators and for every voltage source VS in θ, D and VS are equi-oriented in θ;

(ii) it is: $(I_\theta \neq \varnothing)$ or $(P_\theta \neq \varnothing$ and $N_\theta \neq \varnothing)$

If the set $\mathscr{T}$ is empty, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *closed* state in $\mathbf{s}$.

Proof: Statement (1_a) (resp.: (2_a)) is an immediate consequence of the application of the KVL (resp.: KCL) to the admissible loop (resp.: cut-set) of diodes and nullators: the sum of non-positive voltages (resp.: currents) must be zero, hence all the voltages (resp.: currents) must be zero. Thus, for every $\mathbf{s} \in S(N)$, all the diodes of the admissible loop (resp.: cut-set) are in the closed (resp.: open) state in $\mathbf{s}$.

The proof of Statements (1_b) and (2_b) uses the following *Colored-Branch Theorem*[1]:

Let us consider a partially oriented graph, containing at least one oriented branch. Let each of the oriented branches of the graph be green *colored, let the set of the non-oriented branches be arbitrarily partitioned into two disjoint sets – each one may be empty –, and let the branches of the first of these two sets be* red *colored and those of the second set be* blue *colored.*

Then, each one of the green *colored branches satisfies one of the following two mutually exclusive statements*:

(a) *it is part of a uniform loop*[2] *of* green *and* red *branches*;

(b) *it is part of a uniform cut-set of* green *and* blue *branches.*

Proof of statement (1_b). Let D be a diode of N not part of an admissible loop of diodes and nullators. The statement to prove is equivalent to: *If* there exists $\mathbf{s} \in S(N)$ in which the current in D is positive, *then* the set $\mathscr{M}$ is not empty, i.e.: in N there exists an admissible loop μ such that:

(i) it contains no nullators and for every current source CS in μ, D and CS are equi-oriented in μ;

(ii) it is: $(I_\mu \neq \varnothing)$ or $(P_\mu \neq \varnothing$ and $N_\mu \neq \varnothing)$

Let $\mathbf{s} \in S(N)$ be such that in $\mathbf{s}$ the current in D is *positive*. Let $\mathscr{G}$ be a non-oriented copy of the graph of N. Once numbered the nodes and the branches of $\mathscr{G}$ as those of N, let define a partial orientation of the branches of $\mathscr{G}$ as follows: If the current in the j-th branch of N is positive (resp.: negative) in $\mathbf{s}$, then define the orientation of the j-th branch of $\mathscr{G}$ to be the same of (resp.: the opposite to) the reference direction of the *current* in the corresponding branch of N; If the current in the j-th branch of N is zero in $\mathbf{s}$ then the j-th branch of $\mathscr{G}$ is not oriented. Finally, let the oriented branches of $\mathscr{G}$ be *green* colored, and the non-oriented branches be *blue* colored.

Let δ be the branch of $\mathscr{G}$ corresponding to the branch of N containing D. The branch δ is green colored. By the *Colored-Branch Theorem* applied to $\mathscr{G}$, one of the following two mutually exclusive statements holds: (a) δ is part of a

[1] A proof of the Colored Branch Theorem can be found in [6, Section II] or [10, Theorem 3.1.11].

[2] A *uniform loop* (resp.: a *uniform cut-set*) of a partially oriented graph, is a loop all whose oriented branches have the same orientation in the loop (resp.: in the cut-set).

uniform loop μ' of green branches; (b) δ is part of a uniform cut-set θ' of green and blue branches.

Statement (b) is false, otherwise the KCL applied to θ (the cut-set of N corresponding to θ') would not be satisfied (remember that all the green branches in θ' have the same orientation in the cut-set, and that the current in the branches of N corresponding to the blue branches is zero). Hence, statement (a) holds.

Let μ be the loop of N corresponding to μ'. Obviously, μ is admissible and verifies statement (i). Moreover, since μ is not an admissible loop of diodes and nullators, we have: $P_\mu \cup N_\mu \cup I_\mu \neq \varnothing$ and, since $\mathbf{s} = (\mathbf{i}, \mathbf{v})$ is a solution of N, by the KVL applied to μ it is:

$$\sum_{j \in P_\mu^*} |v_j| - \sum_{j \in N_\mu^*} |v_j| + \sum_{j \in I_\mu^*} (-1)^{\sigma_j} v_j = 0$$

where: P_μ^*, N_μ^* and I_μ^* are the set of the j such that branch j of N is in P_μ, N_μ and I_μ, respectively, and each $\sigma_j \in \{0, 1\}$. Moreover: if $j \in P_\mu^*$ or $j \in N_\mu^*$, then $v_j \neq 0$. Hence the equation above implies:

$$P_\mu \cup I_\mu \neq \varnothing \quad \text{and} \quad N_\mu \cup I_\mu \neq \varnothing$$

and this statement is equivalent to (ii).

Statement (1_b) is proved.

Proof of statement (2_b). Let D be a diode of N not part of an admissible cut-set of diodes and nullators. The statement to prove is equivalent to: *If* there exists $\mathbf{s} \in S(N)$ in which the voltage in D is negative, *then* the set $\mathscr{T}$ is not empty, i.e.: in N there exists an admissible cut-set θ such that:

(i) it contains no nullators and for every voltage source VS in θ, D and VS are equi-oriented in θ;
(ii) it is: ($I_\theta \neq \varnothing$) or ($P_\theta \neq \varnothing$ and $N_\theta \neq \varnothing$)

Let $\mathbf{s} \in S(N)$ be such that in $\mathbf{s}$ the voltage of the diode D is *negative*. Let $\mathscr{G}$ be a non oriented copy of the graph of N. Once numbered the nodes and the branches of $\mathscr{G}$ as those of N, let define a partial orientation of the branches of $\mathscr{G}$ as follows: If the voltage in the j-th branch of N is positive (resp.: negative) in $\mathbf{s}$, then define the orientation of the j-th branch of $\mathscr{G}$ to be the same of (resp.: the opposite to) the reference direction of the *voltage* in the corresponding branch of N; If the voltage in the j-th branch of N is zero in $\mathbf{s}$ then the j-th branch of $\mathscr{G}$ is not oriented. Finally, let the oriented branches of $\mathscr{G}$ be *green* colored, and the non-oriented branches be *red* colored.

Let δ be the branch of $\mathscr{G}$ corresponding to the branch of N containing D. The branch δ is green colored. By the *Colored-Branch Theorem* applied to $\mathscr{G}$, one of the following two mutually exclusive statements holds: (a) δ is part of a uniform loop μ' of green and red branches; (b) δ is part of a uniform cut-set θ' of green branches.

Statement (a) is false, otherwise the KVL applied to μ (the loop of N corresponding to μ') would not be satisfied (remember that all the green branches in μ' have the same orientation in the loop, and that the voltage in the branches of N corresponding to the red branches is zero). Hence, statement (b) holds.

Let θ be the cut-set of N corresponding to θ'. Obviously, θ is admissible and verifies statement (i). Moreover, since θ is not an admissible cut-set of diodes and nullators, we have: $P_\theta \cup N_\theta \cup I_\theta \neq \varnothing$ and, since $\mathbf{s} = (\mathbf{i}, \mathbf{v})$ is a solution of N, by the KCL applied to θ it is:

$$\sum_{j \in P_\theta^*} |i_j| - \sum_{j \in N_\theta^*} |i_j| + \sum_{j \in I_\theta^*} (-1)^{\sigma_j} i_j = 0$$

Moreover: if $j \in P_\theta^*$ or $j \in N_\theta^*$, then $i_j \neq 0$. Hence the equation above implies:

$$P_\theta \cup I_\theta \neq \varnothing \quad \text{and} \quad N_\theta \cup I_\theta \neq \varnothing$$

and this statement is equivalent to (ii).

Statement (2_b) is proved. ■

Remark 2: Linearity of the resistors is not essential in the proof of Theorem 1. Let $\mathscr{P}_+$ (resp.: $\mathscr{P}_-$) be the set of the resistive one-ports such that, assuming associate reference directions for the port voltage v and the port current i, for every v, i in the constitutive relation it is: $vi \geqslant 0$ (resp.: $vi \leqslant 0$) and $vi = 0$ if and only if both $v = 0$ and $i = 0$.[3] Theorem 1 holds for the class of the circuits composed of a finite number of $\mathscr{P}_+$ one-ports, $\mathscr{P}_-$ one-ports, ideal diodes, nullators, norators and independent voltage and current sources.

Moreover, by their topological nature, *the conditions of Theorem 1 are independent of the constitutive relations of the resistors and the positive values of the sources, and the same holds for their consequences.*

III. RDS Circuits

In this section we consider *RDS circuits* i.e. circuits composed of a finite number of positive linear resistors, ideal diodes, and nonzero independent voltage and current sources. For this class of circuits, Theorem 1 can be simplified in the forthcoming Theorem 2, and we can give an additional condition sufficient to determine the state of a diode, formulated as Corollary 1.

The following statement, a slight refinement of Theorem 1 of [7], is simply a reformulation of Theorem 1 above in the case of an RDS circuit.

Theorem 2: Let N be an RDS circuit containing at least one diode, and let D be one of the diodes of N. The following statements hold:

(1_a) *If* D is part of an admissible loop of diodes, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *closed* state in $\mathbf{s}$;
(1_b) Let D be not part of a loop as in (1_a), and let $\mathscr{M}$ be the set of all the admissible loops μ containing D and at least one independent source, and such that:
  (i) For every independent current source CS in μ, it is: D and CS are equi-oriented in μ;
  (ii) If there are no independent current sources in μ, then μ contains:
    (ii_a) at least one independent voltage source VS such that: VS and D are equi-oriented in μ;
    (ii_b) at least one resistor, *or* at least one independent voltage source VS such that VS and D are anti-oriented in μ.

[3] $\mathscr{P}_+$ is the class of the *strictly passive* resistive one-ports.

If the set $\mathscr{M}$ is empty, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *open* state in $\mathbf{s}$;

(2_a) *If* D is part of an admissible cut-set of diodes, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *open* state in $\mathbf{s}$;

(2_b) Let D be not part of a cut-set as in (2_a), and let $\mathscr{T}$ be the set of all the admissible cut-sets θ containing D and at least one independent source, and such that:

(i) For every independent voltage source VS in θ, it is: D and VS are equi-oriented in θ;

(ii) If there are no independent voltage sources in θ, then θ contains:

(ii_a) at least one independent current source CS such that: CS and D are equi-oriented in θ;

(ii_b) at least one resistor, *or* at least one independent current source CS such that CS and D are anti-oriented in θ.

If the set $\mathscr{T}$ is empty, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *closed* state in $\mathbf{s}$.

The following definition allows us to formulate the forthcoming Corollary 1, which provides an additional condition sufficient to determine the state of a diode. Such condition was inspired by Theorem 0 of Duffin's paper [11], and it is more intuitive and less cumbersome – but also less powerful – than that established in the previous Theorem 2.

Definition 2: We say that a diode D of an RDS circuit N is *totally equi-oriented* (resp.: *totally anti-oriented*) if: for every source S of N, the diode D and the source S are equi-oriented (resp.: anti-oriented) in any loop containing both the elements.

Observe that this definition uses only the notion of loop, and that it has the following particularly simple practical meaning: a diode is totally equi-oriented when all the sources push the current in the forward direction of the diode, and it is totally anti-oriented when all the sources push the current in the reverse direction.

Corollary 1: Let N be an RDS circuit containing at least one diode, and let D be one of the diodes of N. The following statements hold:

(1) *If* D is not part of an admissible loop of diodes, and D is totally anti-oriented, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *open* state in $\mathbf{s}$;

(2) *If* D is not part of an admissible cut-set of diodes, and D is totally equi-oriented, *then*, for every $\mathbf{s} \in S(N)$, the diode D is in the *closed* state in $\mathbf{s}$.

Proof: To prove Statement (1), assume D be not part of an admissible loop of diodes. If here exists $\mathbf{s} \in S(N)$ such that in $\mathbf{s}$ the current of the diode D is positive, then by Statement (1_b) of Theorem 2, there exists a loop μ and a source S such that S and D are equi-oriented in μ, hence D is not totally anti-oriented.

To prove Statement (2), assume D be not part of an admissible cut-set of diodes. If here exists $\mathbf{s} \in S(N)$ such that in $\mathbf{s}$ the voltage of the diode D is negative, then by Statement (2_b) of Theorem 2, there exists a cut-set θ and a source S such that S and D are equi-oriented in θ. By Lemma 2 of the Appendix, this last condition is equivalent to the existence in N of a loop μ such that S and D are anti-oriented in μ, i.e.: to be D not totally equi-oriented.

Corollary 1 is proved. ■

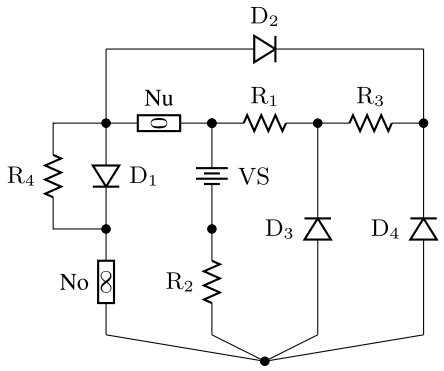

Fig. 5. Circuit N of Example 4.

IV. Examples

In this section, we propose some examples. Examples 3 and 4 show how Theorem 1 can be used to predict the state of the diodes of two simple circuits. In particular, Example 4 shows how the theorem can be used *iteratively*. Example 5 shows how the results of Section III can be used to study a circuit in which, for the diodes, a slightly more complex model than the ideal one has been adopted.

Example 3: Let N be the circuit of Example 2 of Section I, represented in Fig. 3. The circuit contains neither an admissible loop of diodes and nullators, nor an admissible cut-set of diodes and nullators. Hence no one of the diodes satisfies the hypothesis of statement (1_a) or (2_a) of Theorem 1. Instead, D_1 satisfies the hypotheses of statement (1_b) of the same theorem. Indeed, the only admissible loop μ containing D_1 is that composed by D_1, PR and VS. It is $I_\mu = \varnothing$, $N_\mu = \varnothing$ and $P_\mu = \{\text{PR}, \text{VS}\}$ (the voltage source VS and the diode D_1 are anti-oriented in μ). Hence, the set $\mathscr{M}$ relative to D_1 is empty. Then, for every value of the components and every $\mathbf{s} \in S(N)$, the diode D_1 is in the open state in $\mathbf{s}$.

Finally, the diode D_2 satisfies neither the hypotheses of condition (1_b) nor those of condition (2_b). Indeed, D_2 is part of the admissible loop μ composed by D_2, PR, VS, and NR. Hence $I_\mu = \varnothing$, $P_\mu = \{\text{PR}, \text{VS}\}$ and $N_\mu = \{\text{NR}\}$, and the set $\mathscr{M}$ is not empty. Moreover, D_2 is part of the admissible cut-set θ composed by D_2, D_1 and VS. Hence $I_\theta = \{\text{VS}\}$, $P_\theta = N_\theta = \varnothing$, and the set $\mathscr{T}$ is not empty. Thus, Theorem 1 gives no information about the state of D_2.

The actual solutions of N has been found in Example 2 of Section I.

Example 4: Let N be the circuit of Fig. 5. The circuit contains neither an admissible loop of diodes and nullators, nor an admissible cut-set of diodes and nullators. Hence no one of the diodes satisfies the hypothesis of statement (1_a) or (2_a) of Theorem 1. Moreover, it is easy to check by inspection that each of the diodes D_1, D_3 and D_4 satisfies the hypotheses of statement (1_b) of the same theorem (e.g.: the loop μ composed by $\text{D}_4, \text{R}_3, \text{R}_1, \text{VS}, \text{R}_2$ is the unique admissible loop containing D_4, and for such loop it is both $I_\mu = \varnothing$ and

$N_\mu = \varnothing$). Hence, for every value of the components and every $\mathbf{s} \in S(N)$, the diodes D_1, D_3 and D_4 are in the open state in $\mathbf{s}$. Concerning the diode D_2, the hypotheses of statement (1_b) are false by the existence of the loop D_2, R_3, R_1, VS, R_2, No, R_4, and the hypotheses of statement (2_b) are false by the existence of the cut-set D_2, R_1, R_2, No. Hence Theorem 1 gives no information on the state of D_2.

The state of D_2 can be determined by applying Theorem 1 to the circuit obtained from N by *suitably* eliminating D_1, D_3 and D_4, whose state has been determined. Such technique is described by the following statements.

Remark 3: Let N be a circuit containing at least one diode. Using Theorem 1, we can try to predict the state of each of the diodes of N. Let $\mathscr{P}$ be the set of all the diodes of N which satisfy the hypotheses of at least one of the statements (1_a) – (2_b), i.e. the set of all the diodes whose state can be predicted using Theorem 1. The set $\mathscr{P}$ can be partitioned into the union of two disjoint subsets $\mathscr{O}$ and $\mathscr{C}$ – each one may be empty – such that $\mathscr{O}$ (resp. $\mathscr{C}$) contains only diodes whose state has been predicted to be open (resp. closed). Observe that obviously such a partition always exists and it may not be unique. Indeed, a diode may satisfy both hypotheses sufficient to predict its state to be open and hypotheses sufficient to predict its state to be closed.

Definition 3: Let N be a circuit with ρ branches and ν nodes. Let D be a diode of N and n', n'' be the terminal nodes of D.

The circuit obtained from N by *deleting* D is the circuit, with $\rho - 1$ branches and ν nodes, obtained from N by deleting the branch containing D and maintaining the nodes n' and n''. The circuit obtained from N by *contracting* D is the circuit, with $\rho - 1$ branches and $\nu - 1$ nodes, obtained from N by deleting the branch containing D and then identifying the nodes n' and n''.

Lemma 1: Let N be a circuit containing at least one diode, and let $\mathscr{O}$ and $\mathscr{C}$ be two disjoint sets, not both empty, where $\mathscr{O}$ and $\mathscr{C}$ contain diodes of N whose state is known to be *open* and *closed*, respectively, in every $\mathbf{s} \in S(N)$. Finally, let N^* be the *reduced circuit* obtained from N by *deleting* all the diodes in $\mathscr{O}$, and *contracting* all the diodes in $\mathscr{C}$. The following statement holds:

If D is a diode of N^*, and for every $\mathbf{s}^* \in S(N^*)$ the state of D is open (resp.: closed) in $\mathbf{s}^*$, *then* D is a diode of N, and for every $\mathbf{s} \in S(N)$ the state of D is open (resp.: closed) in $\mathbf{s}$.

Proof: Obviously D is a diode of N. The proof of the statement, by contradiction, is obtained using the following easily proved fact: *If* there exists $\mathbf{s} \in S(N)$ in which the current in D is positive (resp.: the voltage in D is negative) *then* there exists $\mathbf{s}^* \in S(N^*)$ in which the current in D is positive (resp.: the voltage in D is negative). ■

Continuation of Example 4: Let N^* be the circuit of Fig. 6, obtained from N (Fig. 5) by deleting the diodes D_1, D_3 and D_4. The circuit contains neither an admissible loop of diodes and nullators, nor an admissible cut-set of diodes and nullators. The diode D_2 satisfies the hypotheses of statement (2_b) of Theorem 1 applied to N^* (observe that the branches D_2, R_1, R_2, No *does not define a cut-set*). Hence, for every value of the components and every $\mathbf{s}^* \in S(N^*)$, the diode D_2 is in the closed state in $\mathbf{s}^*$. By Lemma 1, for every value of the components and every $\mathbf{s} \in S(N)$, the diode D_2 is in the closed state in $\mathbf{s}$.

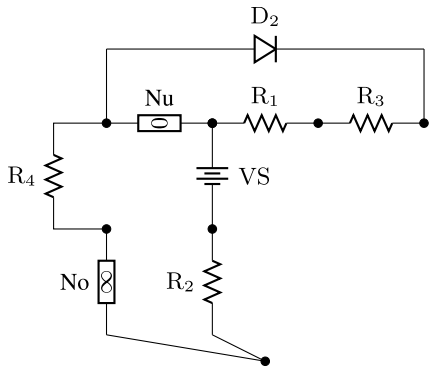

Fig. 6. Circuit N^* of Example 4.

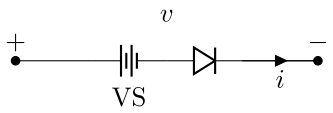

Fig. 7. One-port realization of the constant-voltage-drop model.

Now, to find all the solutions of N it is sufficient to analyse *one* linear circuit instead of the 2^4 required by the elementary procedure: the linear circuit obtained by replacing in N the diodes D_1, D_3 and D_4 by open circuits and D_2 by a short circuit. We conclude that for every value of the components, N has a unique solution, $\mathbf{s}$, and, in $\mathbf{s}$, it is: $v = i = 0$ for both D_1 and D_2, and $v < 0$, $i = 0$ for both D_3 and D_4.

Example 5: The ideal diode is the simplest model for a diode. Many more complex models can be realized by RDS one-ports, hence all the circuits composed of such one-ports, positive linear resistors, negative linear resistors, nullators, norators and independent voltage and current sources, can be studied as circuits composed of positive linear resistors, negative linear resistors, *ideal diodes*, nullators, norators and independent voltage and current sources. Hence, the results of Sections II and III can be applied to circuits in which the diodes are modeled as RDS one-ports.

As an example, let N be a Graetz bridge in which each diode is modeled by the *constant-voltage-drop* model. This model is realized by the RDS one-port of Fig. 7, whose constitutive relation is:

$$v - \Gamma \leqslant 0, \quad i \geqslant 0, \quad (v - \Gamma)\, i = 0$$

where the positive value Γ of VS represents the voltage drop in the forward-conducting diode.

The circuit N above is represented in Fig. 8. The circuit contains neither an admissible loop of diodes, nor an admissible cut-set of diodes, and in every admissible loop μ containing D_2 (resp.: D_4), the diode D_2 (resp.: D_4) and each voltage source contained in μ are anti-oriented. Hence, by statement (1_b) of Theorem 2, for every value of the components and every $\mathbf{s} \in S(N)$ the diodes D_2 and D_4 are in the open state in $\mathbf{s}$. Instead, neither D_1 nor D_3 verify the topological conditions required by Corollary 1 or by Theorem 2.

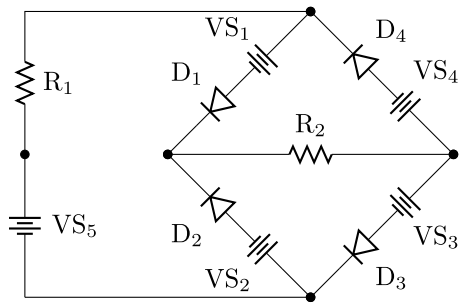

Fig. 8. Circuit N of Example 5.

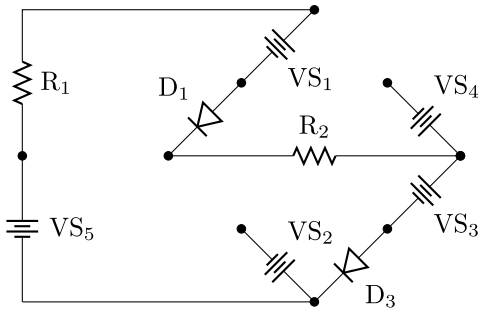

Fig. 9. Circuit N^* of Example 5.

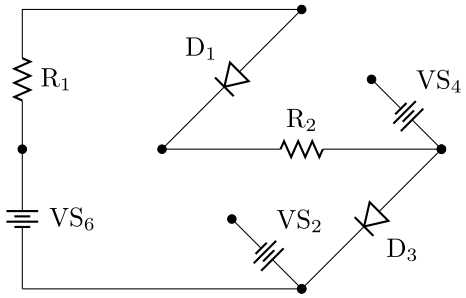

Fig. 10. Circuit M of Example 5.

Hence these statements give no information about the state of D_1 and D_3.

Consider now the circuit N^* of Fig. 9, obtained from N by *deleting* D_2 and D_4, and apply the *v-shift property source transformation* (see [9, Chapter 12, Section 1.1]) to the cut-set VS_1, VS_5 to shift VS_1, and then to the cut-set VS_3, VS_5 to shift VS_3. Finally, replace the series connection of the three sources VS_5, VS_1 and VS_3 by a single source VS_6. The circuit M obtained is represented in Fig. 10. Obviously, as far as it concerns the state of the common diodes, the circuits N^* and M are equivalent.

For every k, let E_k be the value of the voltage source VS_k, so that $E_6 = E_5 - E_1 - E_3$.

If E_1, E_3 and E_5 are such that $E_5 - E_1 - E_3 > 0$, then it is $E_6 > 0$. The circuit contains neither an admissible loop of diodes, nor an admissible cut-set of diodes, and both D_1 and D_3 are totally equi-oriented. Then, by Corollary 1, independently of the value of the components, both diodes are in the closed state in every solution of M, hence in every solution of N.

If E_1, E_3 and E_5 are such that $E_5 - E_1 - E_3 < 0$, then it is $E_6 < 0$. Let M' be the circuit obtained from M by changing the orientation of VS_6. This new circuit contains neither an admissible loop of diodes, nor an admissible cut-set of diodes, and both D_1 and D_3 are totally anti-oriented. Then, by Corollary 1, independently of the value of the components, both diodes are in the open state in every solution of M', hence in every solution of N.

Finally, if E_1, E_3 and E_5 are such that $E_5 - E_1 - E_3 = 0$ then it is $E_6 = 0$. Let M'' be the circuit obtained from M by contracting VS_6. This new circuit contains neither an admissible loop of diodes, nor an admissible cut-set of diodes, and both D_1 and D_3 are *both* totally anti-oriented *and* totally equi-oriented (there is a unique loop, and it contains both diodes and *no sources*). Then, by Corollary 1, independently of the value of the components, both diodes are *both* in the closed state *and* in the open state in every solution of M'', hence in every solution of N. Therefore, for both diodes it is $v = i = 0$.

In each of the above cases, to find all the solutions of N it is sufficient to analyse *one* linear circuit instead of the 2^4 required by the elementary procedure: that obtained by replacing in N the diodes by the suitable combination of open and short circuits.

V. Conclusion

Let N be a circuit composed of a finite number of positive and negative linear resistors, ideal diodes, nullators, norators and nonzero independent current and voltage sources, and let N contain at least one diode, D. We have given some topological conditions sufficient to predict the state of D, i.e. to ensure that for every solution $\mathbf{s}$ of N, the diode D is in the open (resp.: closed) state. We also specialized our conditions to the case of N being an RDS circuit, i.e. a circuit composed of a finite number of positive linear resistors, ideal diodes and nonzero independent current and voltage sources.

In some examples, we have demonstrated how our conditions can be applied, by inspection, to analyse simple circuits. In particular, we have shown how our technique can be iterated, as soon as the state of some diodes has been predicted, by analysing a suitable reduced circuit. In a final example, we have applied our results to analyse a circuit in which the diodes have been modeled by a constant-voltage-drop model.

When N is a more complex circuit, an algorithm must be devised to analyse N using our conditions.

Let us assume to have a procedure, TEST, which operates on a circuit M, containing $m > 0$ diodes, by applying Theorem 1 to each of its diodes, and returns the set $\mathscr{P}$ of the diodes of M whose state has been predicted, partitioned as $\mathscr{P} = \mathscr{O} \cup \mathscr{C}$, where $\mathscr{O}$ (resp. $\mathscr{C}$) contains only diodes whose state has been predicted to be open (resp. closed), as described in Remark 3. Observe that the procedure TEST must check m times the hypotheses of conditions $(1_a) - (2_b)$ of Theorem 1.

An example of algorithm which, to determine the solutions of N, applies the procedure TEST to a suitable sequence $N_1, \ldots, N_t$ of circuits is the following:

Notations used in the algorithm

k: a counter,
N_j: the circuit on which the j-th execution of TEST will operate,
d_j: the number of diodes of N_j,
$\mathscr{P}_j$: the set of diodes of N_j whose state has been predicted applying TEST to N_j,
π_j: the number of elements of $\mathscr{P}_j$,
$\mathscr{O}_j$: the component of the partition of $\mathscr{P}_j$ returned by TEST applied to N_j and containing only diodes whose state has been predicted to be open,
$\mathscr{C}_j$: the component of the partition of $\mathscr{P}_j$ returned by TEST applied to N_j and containing only diodes whose state has been predicted to be closed;

Algorithm

(0) Set $k = 1$ and $N_1 = N$ (N_1 *contains* $d_1 = d > 0$ *diodes*);
(1) Apply the procedure TEST to N_k, denote by $\mathscr{P}_k$ the set returned by TEST, i.e. the set of the diodes of N_k whose state has been predicted, and by $\mathscr{O}_k \cup \mathscr{C}_k$ its partition, let π_k be the number of elements of $\mathscr{P}_k$;
(2) If $\mathscr{P}_k \neq \varnothing$, then:
  (i) if $\pi_k < d_k$ then: construct the reduced circuit N_{k+1} obtained from N_k by deleting all the diodes of $\mathscr{O}_k$ and contracting all the diodes of $\mathscr{C}_k$ (N_{k+1} *contains* d_{k+1} *diodes, where* $0 < d_{k+1} = d_k - \pi_k < d_k$), set $k := k + 1$ and go to step (1);
  (ii) if $\pi_k = d_k$ then go to step (4);
(3) If $\mathscr{P}_k = \varnothing$, then the set of diodes of N whose state has been predicted is:

$$\mathscr{P} = \begin{cases} \text{the empty set}, & \text{if } k = 1 \\ \mathscr{P}_1 \cup \cdots \cup \mathscr{P}_{k-1}, & \text{if } k > 1 \end{cases}$$

which has:

$$p = \begin{cases} 0, & \text{if } k = 1 \\ \pi_1 + \cdots + \pi_{k-1}, & \text{if } k > 1 \end{cases}$$

elements; each diode of $\mathscr{P}$ has now a known state assigned by the previous steps. To find the solutions of N: for each of the 2^{d-p} combinations of states of the $d - p$ diodes of N whose state has not been predicted, execute steps (a) and (b) of the elementary procedure (2^{d-p} *linear circuits must be solved and the algorithm terminates*).
(4) The state of all the diodes of N has been predicted: each diode of N has now a known state assigned by the previous steps. To find the solutions of N, analyse the linear circuit obtained from N by replacing each diode by a short or open circuit as required by the predicted state (*only one linear circuit must be solved and the algorithm terminates*).

Let us observe that:

- The algorithm terminates after at most d executions of TEST.
- The algorithm checks the hypotheses of conditions $(1_a)-(2_b)$ of Theorem 1 *at least* d times, and *at most* $d(d+1)/2$ times.

Indeed: If the algorithm terminates after one execution of TEST, the statement in obvious.
If the algorithm terminates after $t > 1$ executions of TEST, then the procedure TEST has been applied to the circuits $N_1, \ldots, N_t$. Hence, the hypotheses of conditions $(1_a)-(2_b)$ of Theorem 1 have been checked $d_1 + \cdots + d_t$ times. Since $d = d_1 > \cdots > d_t \geqslant 0$, then it is:

$$d \leqslant d_1 + \cdots + d_t \leqslant \sum_{k=0}^{d-1} (d-k) = d(d+1)/2$$

A realization of the algorithm, in particular of the procedure TEST, is currently being studied.

APPENDIX

In this section, we state and prove Lemma 2, used in the proof of Corollary 1.

Lemma 2: Let N be a circuit containing at least one independent source and at least one diode. Let S be an independent source and D be a diode of N.

The statements:

(i) there exists a loop of N in which D and S are equi-oriented
(ii) there exists a cut-set of N in which D and S are anti-oriented

are equivalent, and the statements:

(iii) there exists a loop of N in which D and S are anti-oriented
(iv) there exists a cut-set of N in which D and S are equi-oriented

are equivalent.

Proof: Let $\mathscr{G}$ be a non oriented copy of the graph of N and let δ (resp.: γ) be the branch of $\mathscr{G}$ corresponding to the branch of N containing D (resp.: S). Let δ and γ be oriented as the reference direction of the current in the corresponding branch of N.

Proof of: (i) ⇒ (ii): Let μ be a loop of $\mathscr{G}$ in which δ and γ are equi-oriented. Let the branches δ and γ be green colored, the other branches of μ be red colored, and the remaining branches of $\mathscr{G}$ be blue colored. Let $\mathscr{G}'$ be the partially oriented graph obtained from $\mathscr{G}$ by *inverting the orientation* of the green branch δ. The graph $\mathscr{G}'$ contains a unique loop of green and red branches, but *not* uniform. Hence, by the Colored-Branch Theorem applied to $\mathscr{G}'$, the green branch δ is part of a uniform cut-set θ' of green and blue branches, necessarily containing also γ. The elements D and S are anti-oriented in the cut-set of N corresponding to θ'.

Proof of: (ii) ⇒ (i): Let θ be a cut-set of $\mathscr{G}$ in which δ and γ are anti-oriented. Let the branches δ and γ be green colored, the other branches of θ be blue colored, and the remaining branches of $\mathscr{G}$ be red colored. The graph $\mathscr{G}$ contains a unique cut-set of green and blue branches, but *not* uniform. Hence, by the Colored-Branch Theorem, the green branch δ is part of a uniform loop μ' of green and red branches, necessarily containing also γ. The elements D and S are equi-oriented in the loop of N corresponding to μ'.

Similar arguments prove the remaining equivalence. Lemma 2 is proved. ■

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